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A linear-high range output power control technique for cascode power amplifiers

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ABSTRACT

In this paper a new linear power control technique is presented to control the output power of cascode power amplifiers. Using this technique the output power of power amplifier can be controlled from the maximum output power to −136 dBm, continuously. The characteristic of the output voltage versus control voltage is linear from −15.9 to 18.6 dBm (a range of 34.5 dB) of the output power. Also at this range the Amplitude Modulation to Phase Modulation (AM-PM) distortion is 43°. Furthermore, the input dynamic range is 0.373 V, which is less than the conventional techniques. Having a power controller in a low power path and a low input dynamic range leads to minimizing the controller dissipation and reduction of power added efficiency (PAE). The proposed technique is simulated using 0.13 μm CMOS process model using Advanced Design System and the results obtained are presented.

1. Introduction

Power amplifiers (PAs) are the main consumers of power supply among radio-frequency (RF) blocks. The operating time of a transmitter that uses a limited power supply (such as a battery) is largely dependent on the power consumption of its PA. The lifetime of the battery could be increased if the power consumption of the PA is decreased in unnecessary situations such as idle or standby time.

To reduce the interferences in wireless communication, some limitations are imposed on the transmitted output power in terms of position and distance to the base-station which must be adjustable over a wide power control range (PCR).

The above mentioned factors along with reducing thermal power dissipation in PA are the basic reasons to control the output power of PAs.

Several power control techniques have been presented so far. These techniques have a limited PCR; high phase distortion and/or their AM-AM characteristics (output voltage versus control voltage) are nonlinear [1–4].

Among different structures that are used for power amplifiers, cascode topology is more attractive due to its good operation in high power levels and voltage stress relief on devices [5–9].

This paper introduces a new power control technique. This technique is simulated using 0.13 μm CMOS process model in Advanced Design System, and the results show that the proposed technique supports a wide PCR and linear AM-AM characteristic.

The paper is organized as follows. In Section 2, the main parameters in power control techniques and conventional techniques are explained briefly. In Section 3 advanced power control technique is introduced and compared with conventional power control techniques. The simulation results are presented in Section 4. Finally, in Section 5, conclusions are given.

2. Power control parameters and techniques

There are several parameters in power control techniques, which should be considered. Among them three parameters are more important. These parameters are PCR, Linearity and power added efficiency (PAE).

PCR is the first parameter that is commonly referred to as the maximum range over which the PA output power is controlled. PCR is given by

$$PCR[dB] = P_{OUT,MAX}[dBm] - P_{OUT,MIN}[dBm] \quad (1)$$

where $P_{OUT,MAX}$ and $P_{OUT,MIN}$ are the maximum and the minimum output power, respectively. It is essential to have a wide PCR up to its maximum possible extent that fulfills the need of modern wireless standards, which is more than 30 dB.

The second parameter is linearity that is referred as having a constant slope for AM-AM characteristic. In the linear techniques the amplitude of the output signal of PA can be modulated using power controller itself.

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The third parameter is power added efficiency (PAE), which is the most important parameter in all power amplifiers and is defined as

$$PAE(\%) = \frac{P_{OUT} - P_{IN}}{P_{DC} + P_{DRV}} \times 100 \quad (2)$$

where P_{IN}, P_{OUT}, P_{DC} and P_{DRV} are input RF power to the driver stage, output RF power from PA, DC power dissipated by PA and DC power dissipated by the driver stage, respectively.

To the author's knowledge, there have been two main approaches to continuously control the PA output power, which are supply voltage power control technique (SVPCT) and cascode power control technique (CPCT) [3,4].

In the next sections SVPCT and CPCT are explained briefly and their associated advantages and disadvantages are described.

2.1. Supply voltage power control technique (SVPCT)

Fig. 1a illustrates SVPCT technique. In this technique the supply voltage of PA is controlled by an intermediate circuit (controller). This technique provides a low PCR because the voltage of node X cannot exactly reach V_{DD} and zero.

Even if the voltage controller provides a pure zero voltage at node X, there is still some output voltage. The reason of this nonzero output voltage is feed-through. Eq. (3) represents MOS Gate-Drain capacitance in saturation and triode region, respectively:

$$C_{GD} = WC_{OV} \quad (a)$$

$$C_{GD} = \frac{WLC_{OX}}{2} + WC_{OV} \quad (b) \quad (3)$$

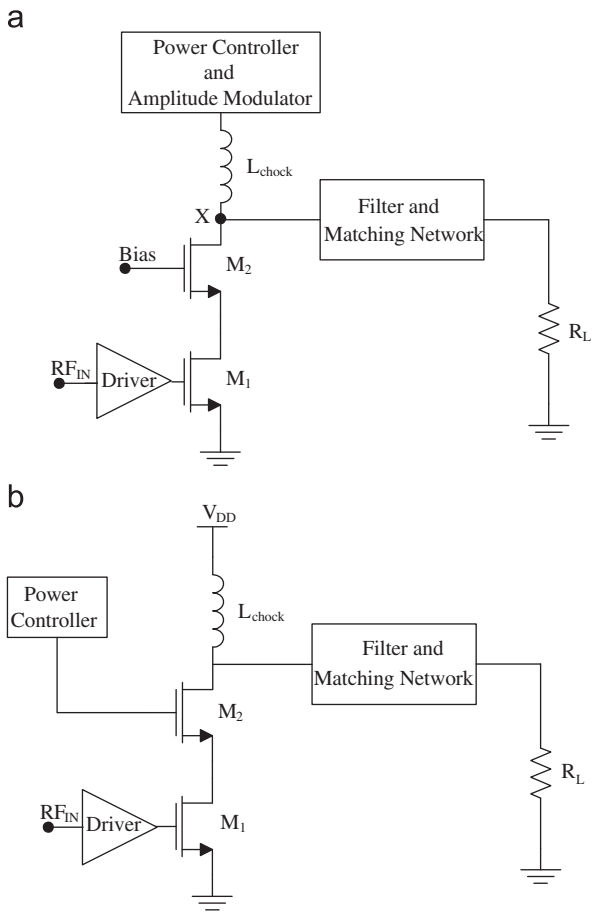

Fig. 1. (a) Supply voltage power control technique and (b) Cascode power control technique.

in which C_{OV} is capacitance due to the overlap of the gate with source and drain areas. From (3) it is clear that C_{GD} increase significantly when MOS operation region goes from saturation to triode. In addition to high gate-drain capacitance, low R_{ON} also leads to feed-through [10]. Fig. 2 shows PCR of SVPCT. Other drawbacks of SVPCT are power controller placement in the high power path and high sensitivity to load variations [11]. For PCR enhancement, Self-Bias SVPCT can be used for simultaneously modifying drain and gate voltage of M_2 [2]. Although Self-Bias improves PCR, it also increases AM-PM distortion to more than 60°. On the other hand, this technique has a large input dynamic range (about 5 V), therefore large power dissipation in controller is generated, which leads to overall PAE of PA reduction.

The main advantage of SVPCT is the linear AM-AM characteristic. Output power for class-E is given by [12]

$$P_{OUT} = 0.577 \frac{V_{DD,PA}^2}{R_L} \quad (4)$$

The output power is also given by

$$P_{OUT} = \frac{V_{OUT}^2}{2R_L} \quad (5)$$

Comparing (4) and (5) shows linear AM-AM characteristic for this technique; that facilitates the power control procedure, besides amplitude modulation becomes practical by the power controller.

2.2. Cascode power control technique (CPCT)

To control the output power of PA, CPCT (Fig. 1b) changes the gate voltage of cascode transistor (M_2) instead of power supply.

Input dynamic range of CPCT is about one threshold voltage lower than SVPCT for the same PCR. The advantage of CPCT is wider PCR compared to SVPCT.

Due to the very small capacitance of drain-source of M_2 in the sub-threshold region, feed-through is reduced (Fig. 3).

The main disadvantage of CPCT is the nonlinear AM-AM characteristic that complicates the power control procedure such that the output power must be adjusted by a feedback or heuristic algorithm (such as neural networks) that needs frequency translation and some other actions (Fig. 4).

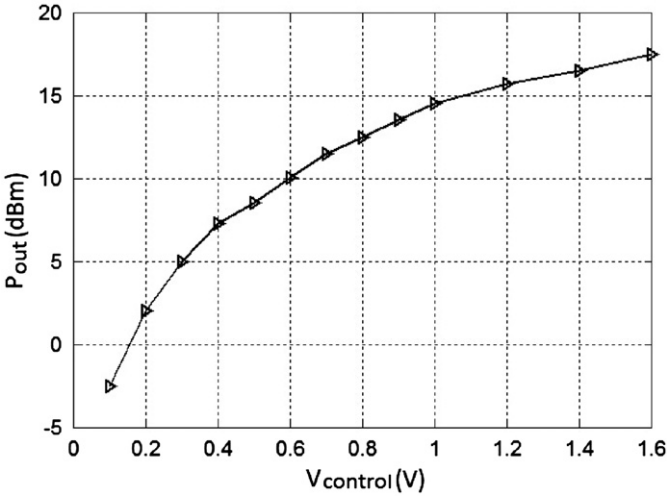

Fig. 2. Output power versus control voltage at SVPCT [4].

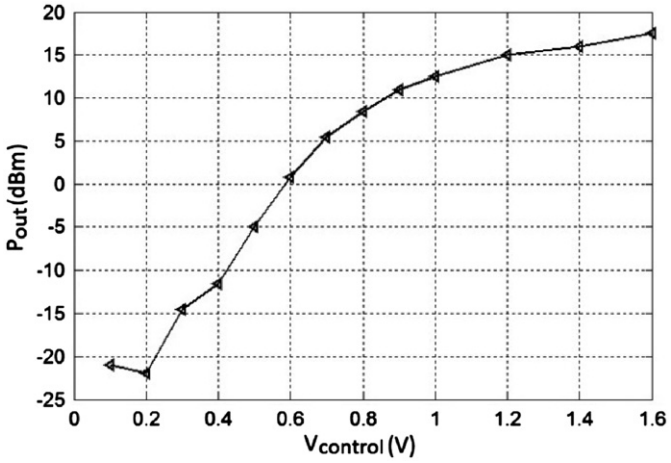

Fig. 3. Output power versus control voltage at CPCT [4].

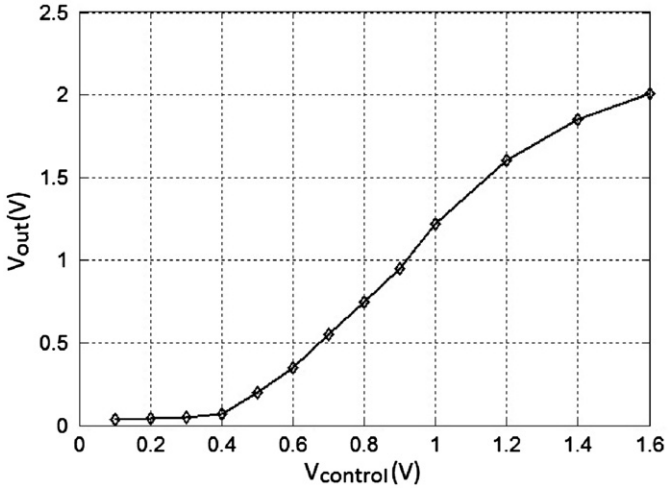

Fig. 4. AM-AM characteristic of CPCT [4].

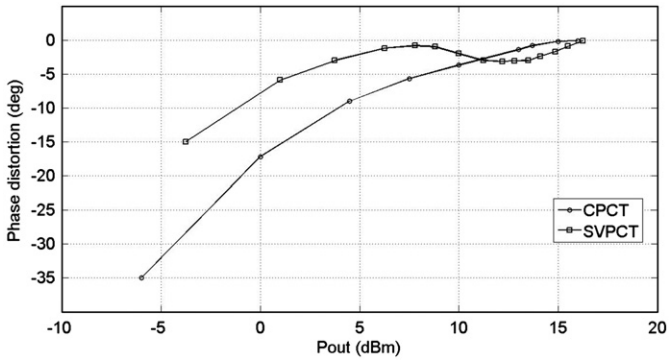

Fig. 5. AM-PM distortion of SVPCT and CPCT [14].

Also AM-PM distortion increased 20° compared to SVPCT due to variation in drain capacitance of M_2 and Miller effect of M_1 gate-drain capacitance [4].

PAE in CPCT is partially better than in SVPCT because the dissipation due to the charge and discharge of parasitic capacitance is reduced [4]. Fig. 5 shows phase distortion of SVPCT and CPCT.

3. Advanced cascode power control technique

Reconsideration of Fig. 4 depicts that the AM-AM characteristic of CPCT can be divided into 3 regions according to the following control voltage intervals:

1- 0.1–0.4 V; the slope of the characteristic is very low;
2- 0.4–1.2 V ; the slope of the characteristic is partly high; and
3- 1.2–1.6 V ; the slope of the characteristic is low.

The three region slopes suggest an increase in first and third part slopes of characteristic to linearize it. By controlling output power of the driver stage, which can be done by applying CPCT to the driver stage, the above linearization is possible. So this technique is named Advanced Cascode Power Control Technique (ACPCT). Fig. 6 illustrates this technique.

In SVPCT and CPCT, PA works in class-E hence the driver output power delivered to PA must be constant and high enough to ensure that the PA works in switching mode. In class-E PAs, for reducing the PA transistor dissipations the width of the transistor channel is increased to some thousand micrometers so as to reduce R_{ON}. Therefore the device input capacitance is increased and the input RF signal cannot be directly applied to PA input. Drivers enhance power of the input RF signal to be suitable for PA. However there is a trade-off between the driver output power level and the PAE of PA. In the medium power levels of PA, an increase in driver output power decreases R_{ON}, which leads to PAE and gain enhancement. But excessive increase raises the driver dissipation without PAE and gain improvement. On the other hand, decreasing the output power of the driver in low power levels causes to change the mode of PA operation from switching mode to linear state and reduction in PAE. Due to this trade-off, we apply a DC-level shift in driver power control path to adapt the driver output power range.

At low control voltages in ACPCT, by decreasing the control voltage the driver output power and therefore the PA output power are decreased. Also, at low control voltages, PA exits from switching mode (class-E) and its output power decreases further. These two phenomena yield high decrease in PA output power with control voltage decrement, which means higher slope of AM-AM characteristic in comparison with CPCT. Besides, at high control voltage levels, by increasing the control voltage (to some extent) the driver output power increases and PA operation approaches an ideal switch (also leads to a reduction in R_{ON}) and consequently its efficiency and output power increase. This means ACPCT AM-AM characteristics have higher slope than CPCT at higher control voltage levels. The two above reasons equalize the slope of the characteristic in three mentioned control voltage regions and linearize it. Unlike CPCT [4], AM-AM characteristic of proposed technique can be described with an exact analytical equation all over of its linear control range:

$$V_{OUT} = \alpha V_{control} + \beta, \quad V_{min} < V_{control} < V_{max} \tag{6}$$

where V_{min} and V_{max} are the lower and upper limits of control voltages in linear range, and V_{out} and $V_{control}$ are amplitudes of output and control voltages, respectively. α and β can be determined simply by simulation or measurement.

The other advantage of ACPCT is its large PCR, although overall this large PCR, AM-AM characteristic is not linear. Decrease in control voltage in ACPCT have two results: (1) PA exits from class-E operation and (2) input power of PA is reduced because CPCT is applied to the driver too. These two results allow ACPCT to decrease its minimum output power significantly, compared to CPCT's one. From an analytical viewpoint, at control voltages below threshold, M_1 and M_3 work in triode region and transconductance of them is small and proportional to their drain-source voltage,

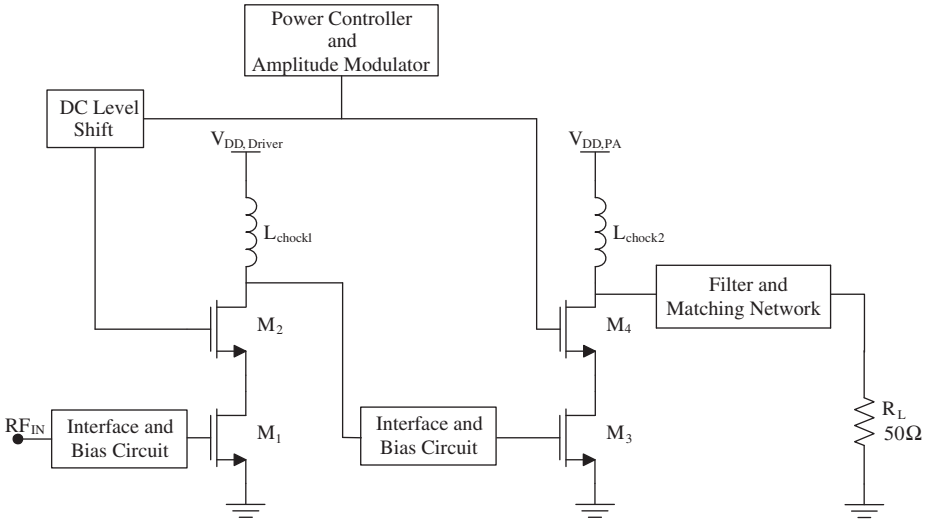

Fig. 6. Advanced Cascode Power Control Technique (proposed technique).

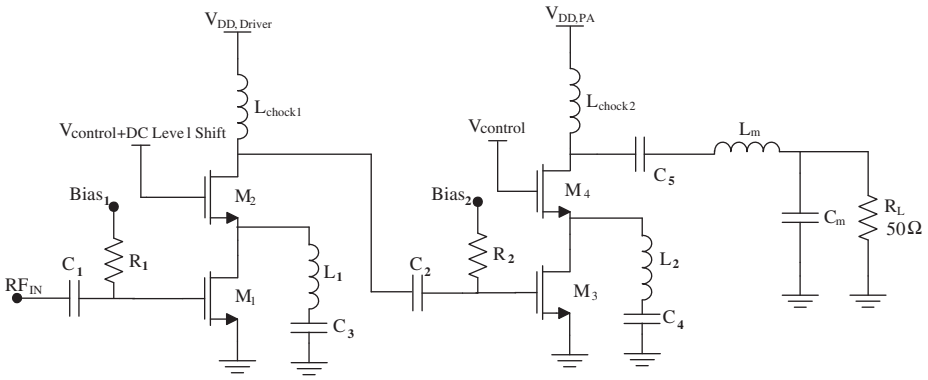

Fig. 7. Circuit schematic of the simulated PA.

Table 1
Circuit component values.

$(W/L)_1$	$(W/L)_2$	$(W/L)_3$	$(W/L)_4$	L_{choke1}
80 μ/0.13 μ	500 μ/0.13 μ	800 μ/0.13 μ	1500 μ/0.1 3μ	2.3 nH
$L_{chocke2}$	L_1	L_2	L_m	C_m
6.6 nH	1.2 nH	2 nH	2.5 nH	2.2 pF

which is also small. On the other hand, M_2 and M_4 work in sub-threshold region and their I/V characteristics are formulated as

$$I_D = I_0 \exp \frac{V_{GS} - V_{TH}}{\xi V_T} \tag{7}$$

where ξ is the nonideality factor, $V_T = KT/q$ and V_{DS} is large enough and its effect is neglected. Eq. (7) says that I_D falls dramatically with decrease in V_{GS}. Since in this region transconductance is directly proportional to I_D, it is also small. Small transconductance of all devices makes it possible to decrease the output power of PA to very small values and therefore the second term in the right hand side of (1) absolutely increases with negative sign, which leads to large PCR for ACPCT in comparison with SVPCT and CPCT. Large PCR makes this technique suitable for standards with very low output power spectral mask.

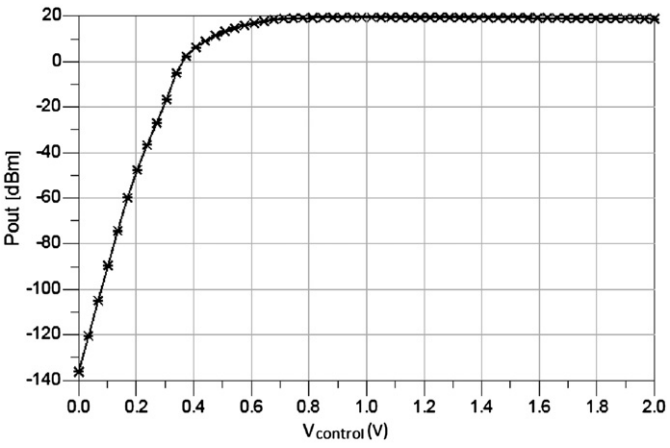

Fig. 8. Output power versus control voltage of the proposed technique.

At low output power values, the PA doesn't work in class-E, so PAE of proposed technique is lower than conventional techniques. At medium output power levels PA works in class-E and driver output power is similar to its counterpart in CPCT, therefore ACPCT's PAE is similar to CPCT. But at high output power levels, the driver output power is higher compared to common class-E PAs and transistors behave more similar to ideal switches. In addition higher control voltages reduce R_{ON} of M_4 and reduce its dissipation. These two

factors increase PAE of the proposed technique in high output power levels in comparison with SVPCT and CPCT.

Since the slope of AM-AM characteristic in ACPCT is higher than CPCT, it's horizontal image is reduced and thereupon input dynamic range is scaled down. AM-PM distortion is originated

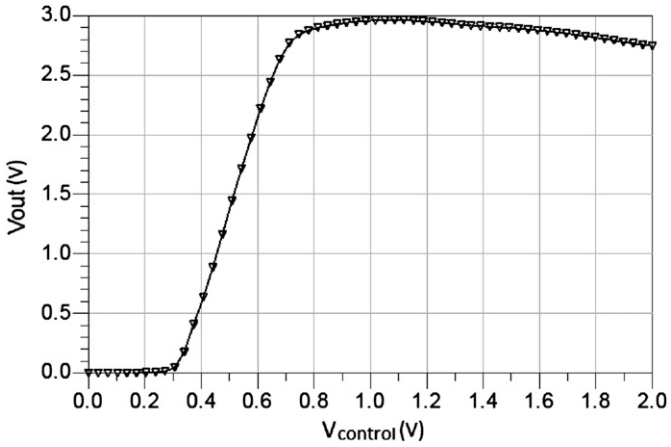

Fig. 9. AM-AM characteristic.

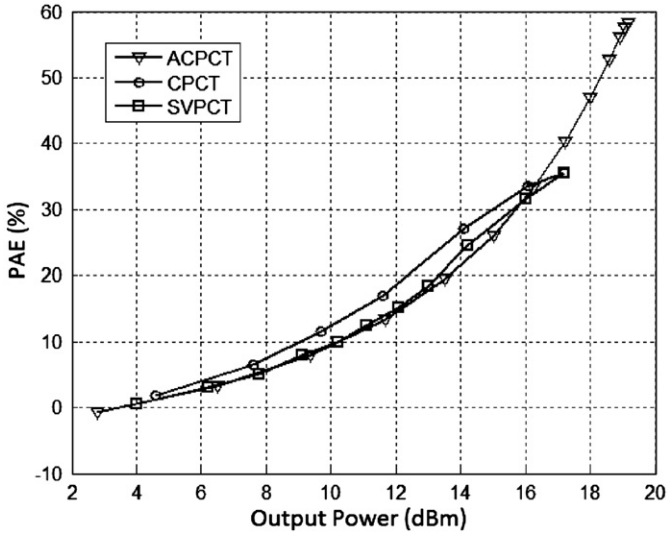

Fig. 10. PAE versus output power [14].

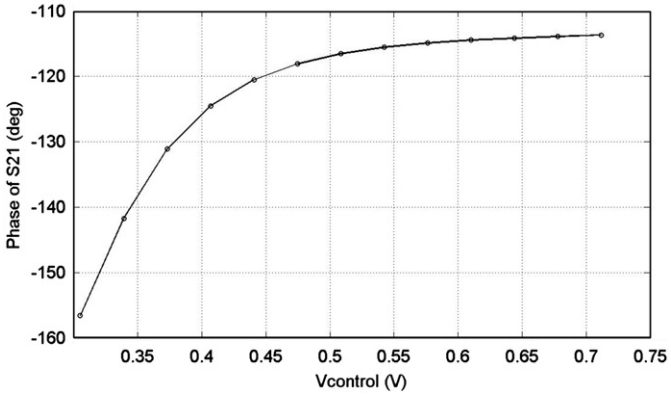

Fig. 11. AM-PM distortion.

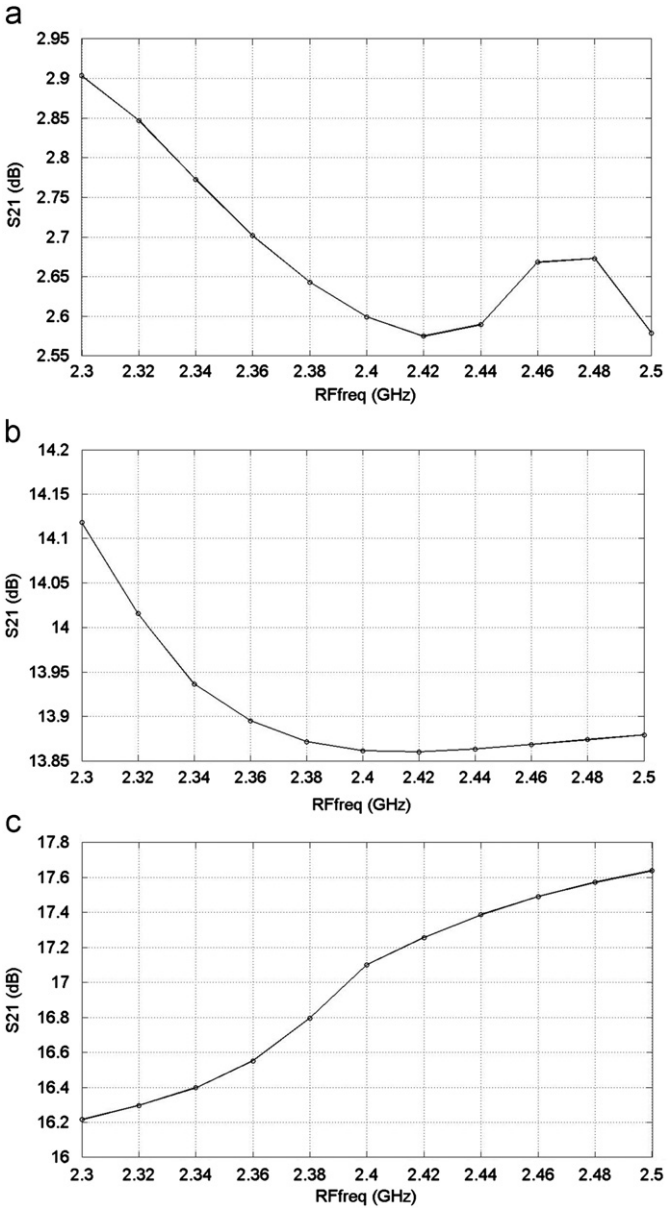

Fig. 12. S_{21} variation in badwidth of operating frequency for three control voltages: (a) 0.4 V, (b) 0.6 V and (c) 0.8 V.

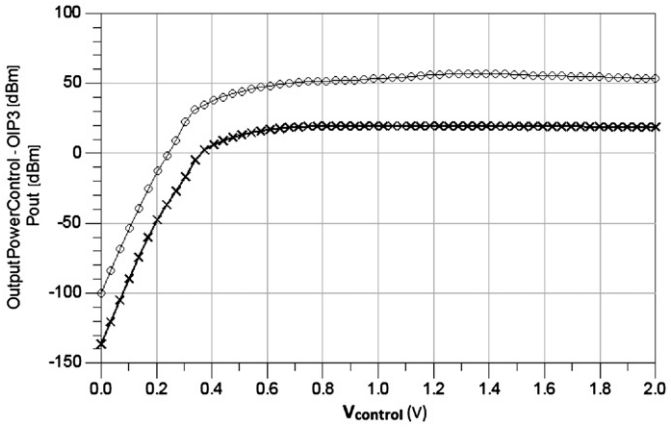

Fig. 13. OIP_3 and output power of PA.

Table 2
Comparison of the selected power amplifiers.

	Technology (nm)	Frequency (GHz)	V_{DD}	*Peak* P_{out} (dBm)	Peak PAE (%)	PCR (dB)	Input dynamic range (V)
Ref. [2]	65	2	5	30	60	34 (Linear) 37 (Nonlinear)	4.9 4.1
Ref. [3]	180	1.9	3.3	32	40	20	2.8
Ref. [4]	180	2.2	1.6	18	35	35	1.4
Ref. [5]	180	2.4	2.4	23	42	–	–
Ref. [13]	350	2.4	1.0	18	33	–	–
This work[a]	**130**	**2.4**	**2.0**	**18.6**[b] **19**[c]	**53** **57**	**34.5** **155**	**0.373** **0.8**

[a] Simulation results.
[b] Linear.
[c] Nonlinear.

from the inverse PN junction capacitance variation with reverse bias voltage on P–N junction.

In ACPCT, CPCT is also applied to the driver; therefore capacitances variation and AM-PM distortion are increased. However owing to the input dynamic range reduction in ACPCT compared with CPCT, capacitances' variation, especially gate-source capacitance of M_4, has smaller value and AM-PM distortion does not increase dramatically compared to CPCT.

4. Simulation and results

Shown in Fig. 7, the proposed technique has been simulated in Advanced Design System using Harmonic Balance and Large-Signal S-Parameter simulators. The device aspect ratios and value of inductors are given in Table 1. Bulk of all devices is grounded. Quality factor of all inductors is set to be 15. Input available power of the driver (P_{IN}) is 3.5 dBm and the operating frequency of the circuit is 2.4 GHz with a bandwidth of 200 MHz. To boost PAE, in both driver and PA stages, an inductor has been added between source of cascode transistor and ground using a capacitor in series to perform DC blocking [6]. In order to input signal of PA be more similar to a square wave, the output signal of driver is directly applied to PA input (without filtering). Gate width of M_4 is selected such that the external capacitor can be eliminated [6]. For output filtering and matching, half-balun circuit, which acts as a low-pass filter ($L_m - C_m$), is used in series with a large capacitor (C_3) for DC blocking. DC level shift is chosen to be 0.1 V to have the maximum AM-AM characteristic linearity.

As shown in Fig. 8, the output power of PA changes between -136 and $+19$ dBm, which means PCR of this technique is 155 dB. Fig. 9 shows AM-AM characteristic of ACPCT. At control voltage range of $0.305-0.678$ V, the characteristic is linear and the maximum slope tolerance is lower than 2.9 dB. The corresponding PCR of this control voltage rang is 34.5 dB (from -15.9 to 18.6 dBm of output power), which is approximately equivalent to CPCT. Input dynamic range corresponding to this PCR is 0.373 V, which is 1.027 and 1.127 V less than CPCT and SVPCT, respectively [4].

Fig. 10 shows the PAE of ACPCT, CPCT and SVPCT. As shown, in the worst case, PAE of ACPCT at 13.8 dBm of PA output power is 7% smaller than CPCT. At high output power where PAE is more important, PAE of the proposed technique is 53% at 18.6 dBm output power (note that maximum PAE is 58% at maximum output power of 19 dBm). These PAEs do not include controller dissipation. The efficiency of power controllers is about 90% at the maximum output power [1]. The placement of controller in CPCT and ACPCT is in low power path, therefore overall PAE of PA and controller in these techniques is better than SVPCT (PAEs shown in Fig. 10 do not include controller dissipation).

Fig. 11 depicts 43° AM-PM distortion of ACPCT in linear PCR, which is 8° more than CPCT. Since power control signal has a very low frequency, this AM-PM distortion does not deteriorate the phase error in the transmitting signal. Also, if phase or frequency modulations are not applied to the signal, the controller can be used for amplitude modulation. However, if controller is intended to be used as amplitude modulator where phase or frequency modulation is also applied to the signal, this AM-PM distortion must be compensated. Shown in Fig. 12, S_{21} variation in frequency bandwidths at 0.4, 0.6 and 0.8 V control voltages are lower than 2 dB, which means flat gain throughout the frequency band. As shown in Fig. 13, OIP_3 of PA at 50 MHz offset frequency is at least 30 dB greater than the output power in overall output power range. It means PA output signal is not distorted by intermodulation components. Performance comparison of proposed PA and traditional ones is shown in Table 2.

5. Conclusion

In this paper a power control technique was presented for cascode power amplifiers. This technique provides a 155 dB power control range. The AM-AM characteristic of PA was linear over a wide output power range of 34.5 dB and facilitates the procedure of power control. The corresponding input dynamic range to linear PCR was 0.373 V that was 1.027 and 1.127 V less than the two conventional techniques (CPCT an SVPCT). The linearity of characteristic makes amplitude modulation possible by power controller where frequency or phase modulations are not applied to the signal. Due to the placement of power controller in the low power path, controller dissipation is minimized. Eliminating feedback circuit of power controller and also amplitude modulator, decreasing circuit complexity and saving chip area are the advantages of this technique. The performance of the proposed technique was tested by simulating a 0.13 μm CMOS power amplifier. Operating at the frequency 2.4 GHz of 200 MHz bandwidth, this PA delivered maximum power of 19 dBm to the load.

References

[1] T.-W. Kwak, M.-C. Lee, G.-H. Cho, A 2 W CMOS hybrid switching amplitude modulator for EDGE polar transmitters, IEEE J. Solid-State Circuits 42 (12) (2007) 2666–2676.
[2] M. Apostolidou, M.-P. Heijden, D.-M.-W. Leenaerts, J. Sonsky, A. Heringa, A Iouri Volokhine, 65 nm CMOS 30 dBm class-E RF power amplifier with 60% PAE and 40% PAE at 16 dB back-off, IEEE J. Solid-State Circuits 44 (5) (2009) 1372–1379.
[3] Ch. Park, Y. Kim, H. Kim, S. Hong, A 1.9 GHz CMOS power amplifier using three-port asymmetric transmission line transformer for a polar transmitter, IEEE Trans. Microw. Theory Tech. 55 (2) (2007) 230–238.

[4] D. Sira, P. Thomsen, T. Larsen, A cascode modulated class-E power amplifier for wireless communications, Microelectron. J. 42 (9) (2011) 141–147.
[5] T Sowlati, D. Leenaerts, A 2.4 GHz 0.18 μm CMOS self-biased cascode power amplifier, IEEE J. Solid-State Circuits 38 (8) (2003) 1318–1324.
[6] S. AnuarZainolMurad, R Pokharel, H. Kanaya, K. Yoshida, O. Nizhnik, A 2.4 GHz 0.18 μm CMOS class-E single-ended switching power amplifier with a self-biased cascode, J. Electron. Commun. 64 (6) (2009) 813–818.
[7] D. Chowdhury, C.-D. Hull, O.-B. Degani, Y. Wang, A.-M. Niknejad, A fully integrated dual-mode highly linear 2.4 GHz CMOS power amplifier for 4 G WiMax applications, IEEE J. Solid-State Circuits 44 (12) (2009) 3393–3402.
[8] O. Degani, F. Cossoy, S. Shahaf, E. Cohen, V. Kravtsov, O. Sendik, D. Chowdhury, C.-D. Hull, S. Ravid, A 90 nm CMOS power amplifier for 802.16e (WiMAX) applications, IEEE Trans. Microw. Theory Tech. 58 (5) (2010) 1431–1437.
[9] Y. Song, S. Lee, E. Cho, J. Lee, S. Nam, A CMOS class-E power amplifier with voltage stress relief and enhanced efficiency, IEEE Trans. Microw. Theory Tech. 58 (2) (2010) 310–317.
[10] Ch. Yoo, Q. Huang, A common-gate switched 0.9 W class-E power amplifier with 41% PAE in 0.25 μm CMOS, IEEE J. Solid-State Circuits 36 (5) (2001) 823–830.
[11] J.N. Kitchen, I. Deligoz, S. Kiaei, B. Bakkaloglu, Polar SiGe class E and F amplifiers using switch-mode supply modulation, IEEE Trans. Microw. Theory Tech. 55 (5) (2007) 845–856.
[12] N.O. Sokal, Class-E power amplifiers, QEX/Commun. Quart. (2001) 9–20.
[13] K.-W. Ho, H.C. Luong, A 1 V CMOS power amplifier for bluetooth applications, IEEE Trans. Circuits Syst.—II 50 (8) (2003) 445–449.
[14] D. Sira, P. Thomsen, T. Larsen, Output power control in class-E power amplifiers, IEEE Microw. Wireless Components Lett. 15 (4) (2010) 232–234.