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Locally one-dimensional finite-difference time-domain scheme for the full-wave semiconductor device analysis

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Abstract: The application of an unconditionally stable locally one-dimensional finite-difference time-domain (LOD-FDTD) method for the full-wave simulation of semiconductor devices is described. The model consists of the electron equations for semiconductor devices in conjunction with Maxwell's equations for electromagnetic effects. Therefore the behaviour of an active device at high frequencies is described by considering the distributed effects, propagation delays, electron transmit time, parasitic elements and discontinuity effects. The LOD-FDTD method allows a larger Courant–Friedrich–Lewy number (CFLN) as long as the dispersion error remains in the acceptable range. Hence, it can lead to a significant time reduction in the very time consuming full-wave simulation. Numerical results show the efficiency of the presented approach.

1 Introduction

Global modelling of mm-wave circuits is an accurate method which considers the distributed effects, parasitic elements and discontinuities. The main issue of this modelling is the full-wave analysis of their active devices (ADs). The equations that describe the transport physics in conjunction with Maxwell's equations must be solved in an accurate analysis to predict the interactions between the carriers and the propagating wave inside the devices [1, 2]. A number of different approaches for the simulation of semiconductor devices have been developed in the past. Most of these techniques are fundamentally dependent upon the solution of the Poisson equation along with the basic carrier transport equations. In this paper, the semiconductor analysis is based on the time-domain drift-diffusion model (DDM) [3]. The set of DDM equations contains the Poisson equation and the carrier transport equations, obtained by splitting the Boltzmann transport equation (BTE) into its first two moments. The DDM model assumes that the carrier temperature is equal to the semiconductor lattice temperature. Therefore the carrier velocity is only dependent on the electric field. In comparison with the other more rigorous techniques, the DDM is a relatively simple one with better convergence of the algorithm and shorter computational time for the numerical modelling of semiconductor devices. Thus, it is more suitable for a design engineer to use for first steps. Another more accurate model can be used to improve the final structure.

Even for simple semiconductor equations, the common FDTD simultaneous simulation of those and Maxwell's equations is very time consuming because of the Courant–Friedrich–Lewy (CFL) stability condition on the simulation time-step size [1, 2]. Recently, a new implicit method, called the locally one-dimensional finite-difference time-domain (LOD-FDTD) method, has been introduced to solve Maxwell's equations [4–7]. This method is an attractive alternative to the standard FDTD because of its unconditional stability with moderate computational overhead. The ADI-FDTD and LOD-FDTD methods can particularly useful for problems involving devices with fine geometric features that are much smaller than the wavelengths of interest [8], as they are free of CFL limit. However, LOD-FDTD presents a better computational efficiency than the ADI-FDTD [9].

This paper presents a semi-implicit numerical method to solve the DDM equation based on the LOD-FDTD scheme. Then, using the LOD-FDTD method for the electromagnetic (EM) equations as well, an unconditionally stable method for the full-wave simulation of semiconductor devices is presented to remove the CFL limit of time-step size. The simulation results show the efficiency of LOD-FDTD method with respect to the conventional FDTD and ADI-FDTD methods.

2 AD model of transistor

For a MESFET as a unipolar microwave/mm transistor, the equations of the DDM are [3]

$$\nabla^2\phi = -\frac{\rho}{\varepsilon} = -\frac{q(N_d^+ - n)}{\varepsilon_0\varepsilon_r} \tag{1}$$

$$\partial_t n = \frac{1}{q}\nabla\cdot\boldsymbol{J}_n = \frac{1}{q}(\partial_x J_x + \partial_y J_y) \tag{2}$$

$$\boldsymbol{J}_n = qn\mu_n(\boldsymbol{E}, N_d)\boldsymbol{E} + qD_n(\boldsymbol{E}, N_d)\nabla n \tag{3}$$

$$\boldsymbol{E} = -\nabla\phi \tag{4}$$

where ϕ is the potential, N_d is the doping profile, n is the electron (carrier) density, μ_n is the mobility coefficient, $D_n = \mu_n K_b T/q$ and ∂_α is the derivative with respect to α. In this work, electron mobility is considered as a function of doping and electric field [10]

$$\mu_n(E, N_d) = \frac{\mu_0 + (v_s/E)(E/E_s)^4}{1 + (E/E_s)^4} \tag{5}$$

whereas low-field mobility μ_0, saturation velocity v_s, and critical field E_s (for the onset of negative differential mobility) are functions of doping N_d.

To have a numerically stable estimation of the electron concentration between nodes, we use the following equation [11, 12] in both x and y directions

$$n(c) = \{1 - g(c, \phi)\}n(a) + g(c, \phi)n(b); \quad a \le c \le b \tag{6}$$

where

$$g(c, \phi) = \frac{1 - e^{CV}}{1 - e^{V}}, \quad V = \frac{(\phi_b - \phi_a)q}{KT}, \quad C = \frac{c - a}{b - a} \tag{7}$$

Using the carrier concentration $n_{i,j}$ at $t = k\Delta t$, (1) can be discretised as

$$\frac{\phi_{i+1,j} - 2\phi_{i,j} + \phi_{i-1,j}}{(\Delta x^2)} + \frac{\phi_{i,j+1} - 2\phi_{i,j} + \phi_{i,j-1}}{(\Delta y^2)} = -\frac{q(N_d^+ - n_{i,j}^k)}{\varepsilon} \tag{8}$$

The time-step size, Δt, in a conventional explicit numerical method for the simulation of semiconductor equations is limited by the average carrier velocity v_d and the spatial step sizes Δx and Δy. The following CFL condition must be applied to obtain the stability and numerical dispersion requirements [8]

$$v_d\Delta t \le [\Delta x^{-2} + \Delta y^{-2}]^{-1/2} \tag{9}$$

We propose to use the LOD-FDTD method, which eliminate the constraints of (9) as follows. By applying the LOD principle [13], the FDTD marching from the kth time-step to the $(k + 1)$th time-step is broken into two computational sub-advancements: the advancement from the kth time-step to the $(k + 1/2)$th one and the advancement from the $(k + 1/2)$th time-step to the $(k + 1)$th one [14]. More specifically, two sub-steps are as follows.

2.1 First step of LOD-FDTD for DDM

In the first step, that is at the $(k + 1/2)$th time step, the first partial derivative on the right-hand side (RHS) of (2), $\partial J_x/\partial x$, is replaced with the average of explicit and implicit difference approximation of its known and unknown pivotal values at the kth and $(k + 1/2)$th time step, whereas the second partial derivatives on the RHS of (2), $\partial J_y/\partial y$, is removed. Using the first-order upwind scheme for the spatial derivatives

$$v\partial_x f(x)|_{x=x_i} = \begin{cases} v_i(f_i - f_{i-1})/\Delta x & \text{if } v_i \ge 0 \\ v_i(f_{i+1} - f_i)/\Delta x & \text{if } v_i < 0 \end{cases} \tag{10}$$

and defining

$$\alpha_i^x = \frac{V_i^x/2}{\Delta x \sinh(V_i^x/2)}, \quad \alpha_j^y = \frac{V_j^y/2}{\Delta y \sinh(V_j^y/2)}$$
$$V_i^x = \frac{\phi_{i,j} - \phi_{i-1,j}}{KT/q}, \quad V_{yi} = \frac{\phi_{i,j} - \phi_{i,j-1}}{KT/q} \tag{11}$$

yield the following equation

$$-A_1 n_{i+1,j}^{k+1/2} + (1 + A_2)n_{i,j}^{k+1/2} - A_3 n_{i-1,j}^{k+1/2} = A_1 n_{i+1,j}^k + (1 - A_2)n_{i,j}^k + A_3 n_{i-1,j}^k \tag{12}$$

where

$$A_1 = \frac{\Delta t D_{i+1j}}{2\Delta x^2} + \frac{\Delta t\mu_{i+1j}\alpha_{i+1}^x(|E_x| + E_x)}{4\Delta x} \tag{13}$$

$$A_2 = \frac{\Delta t D_{ij}}{\Delta x^2} + \frac{\Delta t\mu_{ij}(\alpha_{i+1}^x + \alpha_i^x)|E_x|}{4\Delta x} + \frac{\Delta t\mu_{ij}}{2}\frac{\partial^2\phi}{\partial x^2} \tag{14}$$

$$A_3 = \frac{\Delta t D_{i-1j}}{2\Delta x^2} + \frac{\Delta t\mu_{i-1j}\alpha_i^x(|E_x| - E_x)}{4\Delta x} \tag{15}$$

2.2 Second step of LOD-FDTD for DDM

The second step, that is at the $(k + 1)$th time step, is similar to the first time step except that the y term is used instead of x term. Therefore the first-order upwind discretisation of spatial derivative results in the following equation

$$-B_1 n_{i+1,j}^{k+1/2} + (1 + B_2)n_{i,j}^{k+1/2} - B_3 n_{i-1,j}^{k+1/2} = B_1 n_{i+1,j}^k + (1 - B_2)n_{i,j}^k + B_3 n_{i-1,j}^k \tag{16}$$

where

$$B_1 = \frac{\Delta t}{2\Delta y^2}D_{ij+1} + \frac{\Delta t\mu_{ij+1}\alpha_{j+1}^y(|E_y| + E_y)}{4\Delta y} \tag{17}$$

$$B_2 = \frac{\Delta t}{\Delta y^2}D_{ij} + \frac{\Delta t\mu_{ij}(\alpha_{j+1}^y + \alpha_j^y)|E_y|}{4\Delta y} + \frac{\Delta t\mu_{ij}}{2}\frac{\partial^2\phi}{\partial y^2} \tag{18}$$

$$B_3 = \frac{\Delta t}{2\Delta y^2}D_{ij-1} + \frac{\Delta t\mu_{ij-1}\alpha_j^y(|E_y| - E_y)}{4\Delta y} \tag{19}$$

Fig. 1 shows the flowchart of LOD-FDTD sequence for solving the DDF model. It is significant to indicate that the symmetric and tridiagonal coefficient matrixes for the system of linear equations (12) and (16) are advantageous over, for example, a full Crank–Nicholson scheme. The

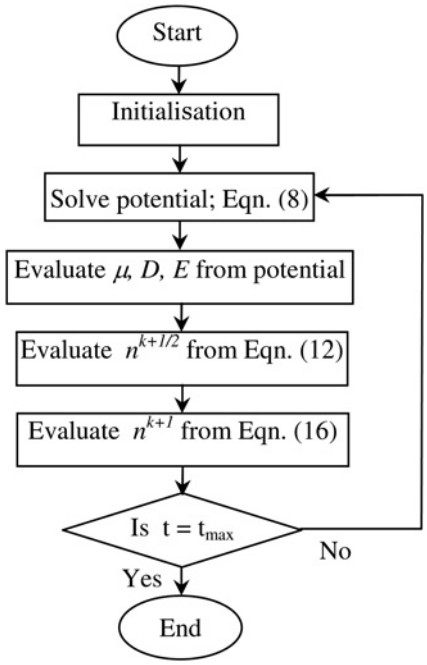

Fig. 1 *Flowchart of the sequence of LOD-FDTD scheme for the DDM*

smaller bandwidths of LOD methods make the system easy to solve by methods such as Choleski decomposition [15].

3 EM model of transistor

Maxwell's equations characterise EM wave propagation completely, which can be written in a matrix form as

$$\partial_t W = (A - B)W + J \tag{20}$$

where

$$W = \begin{bmatrix} E_x & E_y & E_z & H_x & H_y & H_z \end{bmatrix}^{\mathrm{T}}$$
$$J = \begin{bmatrix} J_x & J_y & J_z & 0 & 0 & 0 \end{bmatrix}^{\mathrm{T}}$$
$$A = \begin{bmatrix} \mathbf{0} & A_1/2\varepsilon \\ A_2/2\mu & \mathbf{0} \end{bmatrix}, \quad B = \begin{bmatrix} \mathbf{0} & A_2/2\varepsilon \\ A_1/2\mu & \mathbf{0} \end{bmatrix} \tag{21}$$
$$A_1 = \begin{bmatrix} 0 & 0 & \partial_y \\ \partial_z & 0 & 0 \\ 0 & \partial_x & 0 \end{bmatrix}, \quad A_2 = \begin{bmatrix} 0 & \partial_z & 0 \\ 0 & 0 & \partial_x \\ \partial_y & 0 & 0 \end{bmatrix}$$

In the above equations, E and H are electric and magnetic fields, respectively, and the total current density, J, is calculated by (3) in our problem. To solve (20), LOD-FDTD scheme is used to eliminate the constraints of the CFL condition

$$v_{P\max}\Delta t \le [\Delta x^{-2} + \Delta y^{-2} + \Delta z^{-2}]^{-1/2} \tag{22}$$

in the standard FDTD scheme [8]. In the above equation, $v_{P\max}$ is the maximum of wave phase velocity within the model. In the LOD scheme, (16) is broken into two time steps at $n + 1/2$ and $n + 1$ as

$$(I - A)W^{n+1/2} = (I + A)W^n + 0.5J^n \tag{23}$$

$$(I + B)W^{n+1} = (I - B)W^{n+1/2} + 0.5J^{n+1/2} \tag{24}$$

4 Computational procedure

In each time step, Maxwell's and semiconductor equations should be solved sequentially. The coupling between two models is established by properly transforming the physical parameters (e.g. fields and current densities) from one model to the other. First, Maxwell's equations are solved for the electric and magnetic field distributions using the current density obtained in the previous time step. Then, the obtained EM fields are used in the semiconductor equations to find the new current density. This process is repeated for each time interval [1].

4.1 Transistor simulation

In the following sections, a GaAs MESFET transistor is considered as shown in Fig. 2. As the system of equations for AD and EM models must be solved simultaneously, the cell size is chosen equal to 0.01 μm for x and y directions and 1 μm for the z direction. From (9), (22) and the above cell sizes, the time-step size for explicit FDTD method must be chosen <0.01 fs. Using the implicit LOD-FDTD method for solving both AD and EM equations removes the time-step size limitation. Therefore the time-step size can be selected >0.01 fs. Although the implicit method is unconditionally stable, the time-step size is limited by the numerical dispersion accuracy, as presented in [7]. The full-wave analysis procedure includes two parts as follows.

4.1.1 Steady-state DC solution (initialisation): The steady-state DC solution for the electric fields, current densities and other transport parameters are obtained from the semiconductor model by solving Poisson's and hydrodynamic transport equations. The device is biased and the DC parameter distributions (E, n, ϕ, and J_{dc}) are obtained by solving (3), (4), (12) and (16) until they reach the steady state. This DC solution serves as the corresponding initial values inside the AD model.

The device is biased to $V_{ds} = 2$ V and $V_{gs} = -0.5$ V. The state of the MESFET under DC steady state is represented by the distribution of potential and carrier densities. It is to be noted that Dirichlet boundary condition is used at the electrodes whereas Neumann's boundary condition is used at the other walls. Using the LOD-FDTD method, DC

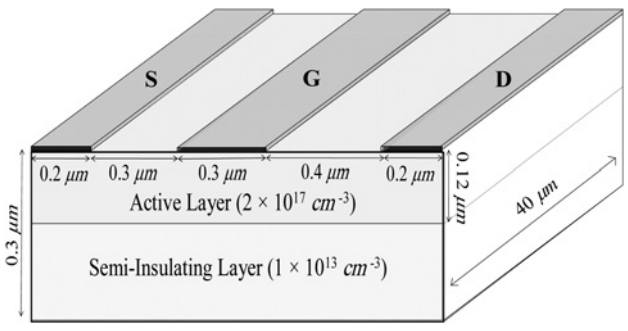

Fig. 2 *Simulated MESFET structure*

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potential and carrier density distributions are obtained as shown in Figs. 3 and 4, respectively. A comparison between results of explicit, ADI and LOD-FDTD methods are provided in Figs. 5 and 6. It is significant to indicate that different methods give precisely the same results and for our 2D problem, the ADI and LOD approaches have a very close performance. In this case, the Courant–Friedrich–Lewy number (CFLN) is defined as the ratio between the time-step size of the 2D unconditionally stable method and the maximum allowable time-step size of the conventional 2D FDTD method from (9). Fig. 7 shows L_2 norm, that is $\|\delta\|_2$, of the relative error in charge density $n_{\{\text{ADI or LOD}\}-\text{FDTD}}$ as a function of the CFLN, whereas using FDTD as the reference

$$|\delta|_2 = \sqrt{\frac{\sum (n_{\{\text{ADI or LOD}\}-\text{FDTD}} - n_{\text{FDTD}})^2}{\sum (n_{\text{FDTD}})^2}} \qquad (25)$$

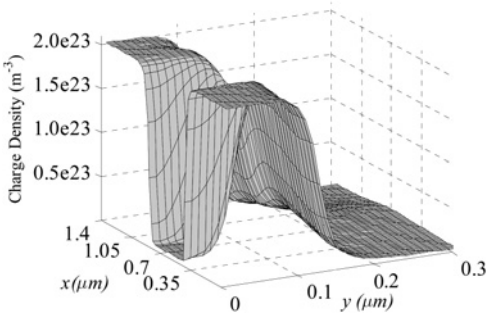

Fig. 3 *Carrier density distribution from LOD-FDTD DC simulation*

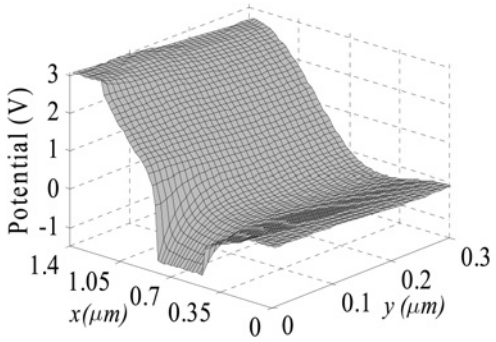

Fig. 4 *Potential distribution from LOD-FDTD DC simulation*

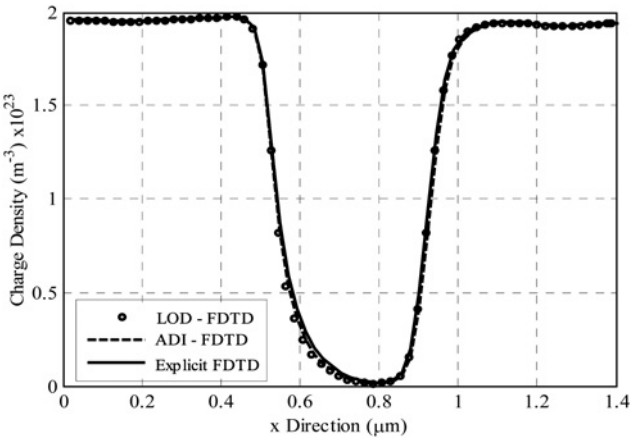

Fig. 5 *Charge density across the 'x' direction at 'y = 0.09 μm'*

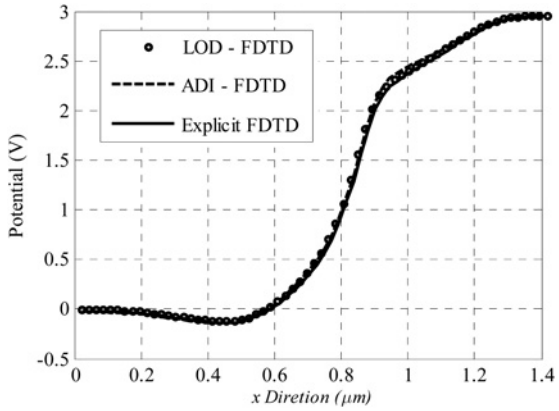

Fig. 6 *Potential distribution across the 'x' direction at 'y = 0.09 μm'*

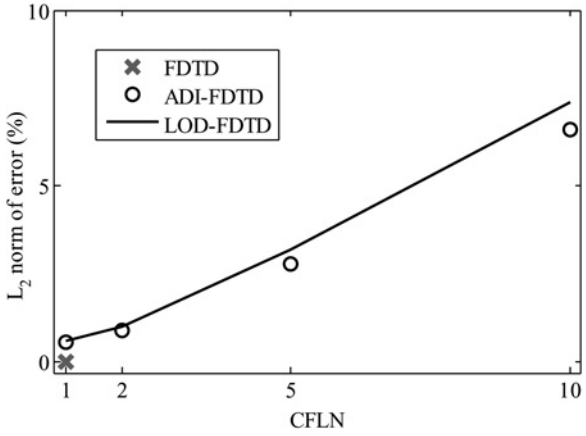

Fig. 7 *L_2 norm of the error of charge density as a function of the CFLN*

4.1.2 Time-domain AC solution: After completing initialisation, the AC excitation is applied, that is, $J = J_{DC} + J_{AC}$. Then, the time-domain distribution of EM fields is obtained from Maxwell's equations. These fields are used by the AD model to update the current density. Fig. 8 shows the sequence's flowchart of this full-wave simulation.

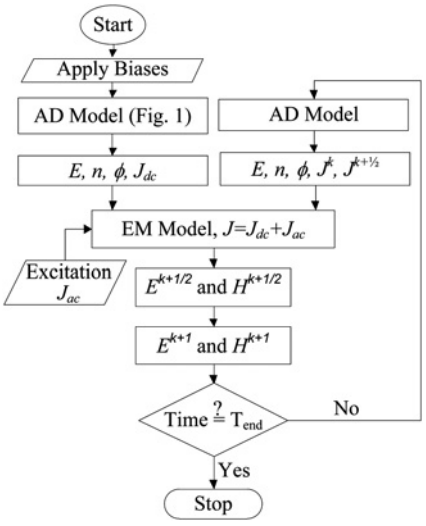

Fig. 8 *Flowchart of the sequence of LOD-FDTD scheme for the DDM*

Since AC simulation contains EM wave propagation, PML absorbing boundary condition is considered in the EM simulation part. The boundary conditions for the AD part of the simulation are same as the boundary conditions in the DC simulation. The AC excitation is applied to the gate electrode, which is given as $V_{gs}(t) = V_{gs0} + \Delta v_{gs}\sin(\omega t)$, where V_{gs0} is DC bias applied to the gate electrode, ω is the frequency of applied signal (100 GHz) and Δv_{gs} is the peak value of AC signal (0.1 V). Fig. 9 shows the output drain voltage obtained by multiplying the total current by the resistance that defines the DC operating point of the transistor [16]. As it can be seen, the results in the conventional, ADI- and LOD-FDTD methods are in good agreement. Fig. 10 shows L_2 norm of the error of output drain voltage as a function of the CFLN ($=\Delta t_{\{\text{ADI or LOD}\}\text{FDTD}}/\Delta t_{\text{FDTD}}$).

Relative speeds of the ADI- and LOD-FDTD methods as the function of CFLN are shown in Fig. 11. For example, when CFLN is equal to 1000, the number of simulation time-steps in implicit cases is reduced by factor 1000 with respect to the explicit case. However, the simulation time of one time-step in our ADI and LOD programmes are approximately equal to the simulation time of five and four time-steps in the FDTD programme, respectively. In this case, the total number of simulation time-steps are 2×10^6, 2×10^3 and 2×10^3 with the approximately simulation times of 24 days, 4 and 3.3 h for the explicit, ADI and LOD FDTD methods, respectively. A PC with a Pentium 4 processor (2.5 GHz) and 2-GB RAM was used in these simulations.

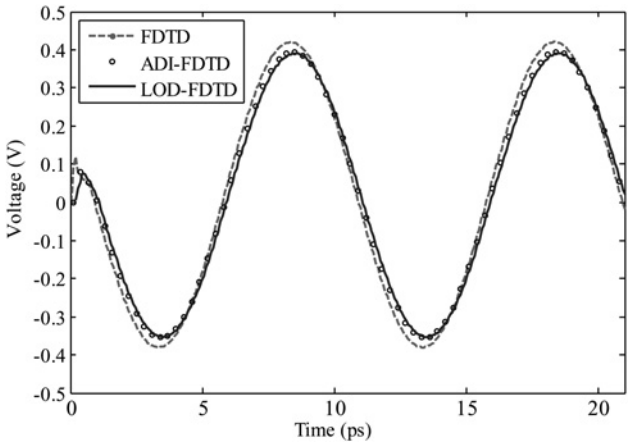

Fig. 9 *Output drain voltage from explicit FDTD ($\Delta t = 0.01$ fs), ADI-FDTD ($\Delta t = 10$ fs), and LOD-FDTD ($\Delta t = 10$ fs) methods*

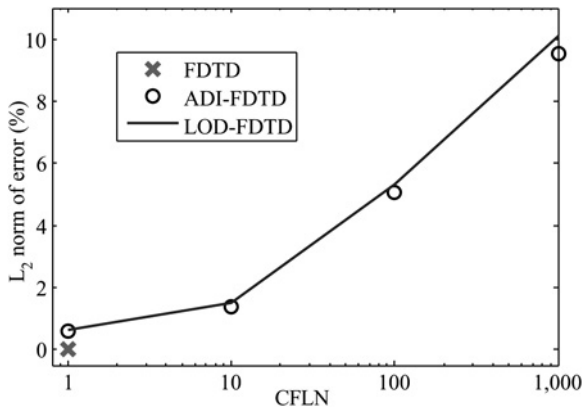

Fig. 10 *L_2 norm of the error of output drain voltage as a function of the CFLN*

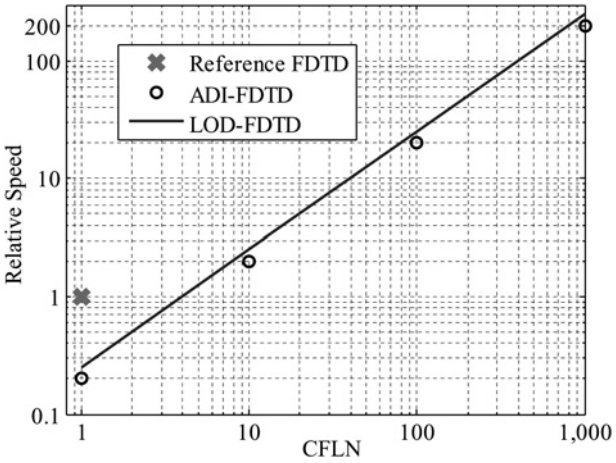

Fig. 11 *Relative speed of the ADI-FDTD and LOD-FDTD methods as a function of the CFLN*

The numerical dispersion error, that is $1 - v_p/c$, of the ADI-FDTD and LOD-FDTD methods is a function of the time-step size and mesh resolution (wavelength per cell size) where v_p/c is the normalised numerical phase velocity [7, 17]. The maximum dispersion error of the ADI-FDTD and LOD-FDTD methods as a function of the CFLN is presented in Fig. 12. As can be seen, the numerical results obtain worse when time-step increases.

4.2 Two-finger MESFET transistor

A two-finger MESFET transistor is considered as the second example. Fig. 13 shows a 3D view of the two-finger simulated transistor [8] with physical parameters in Table 1. The simulated device is biased to $V_{ds} = 3$ V and $V_{gs} = -0.2$ V. A sinusoidal signal is employed in the AC simulations with a peak value of 100 mV and frequency of 100 GHz. This signal is applied between the gate and the source electrodes. The excitation is considered as a plane source at $z = 0$, as shown in Fig. 13. The space and time discretisation parameters are chosen similar to the previous example. Fig. 14 shows the temporal evolution of the output voltage at different sections along the z direction. The output voltage means the voltage signal between the drain and the

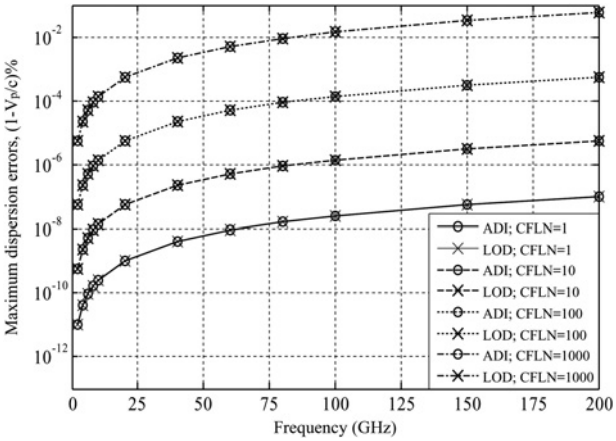

Fig. 12 *Maximum dispersion error of the ADI-FDTD and LOD-FDTD methods as a function of the CFLN and frequency*

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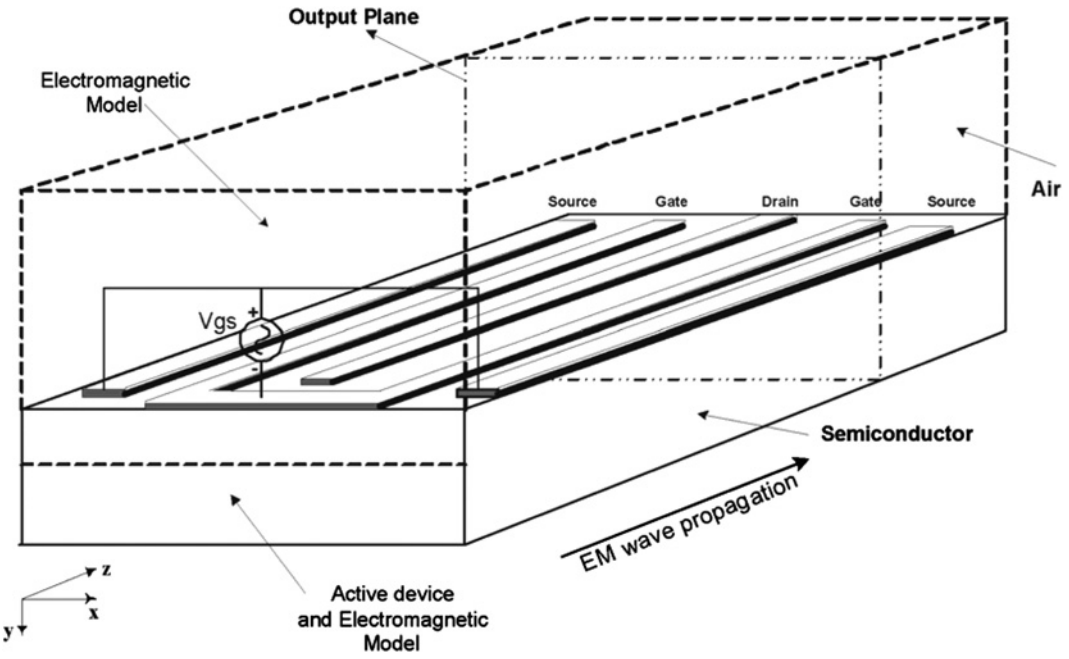

Fig. 13 *Simulated two-finger MESFET structure*

Table 1 Two-finger MESFET transistor parameters

Parameter	Value
drain and source contact lengths	0.5 m
gate–source separation	0.5 m
gate–drain separation	0.45 m
device thickness	0.4 m
gate length	0.25 m
device width	150 m
active layer thickness	0.12 m
active layer doping	2×10^{17} cm^{-3}

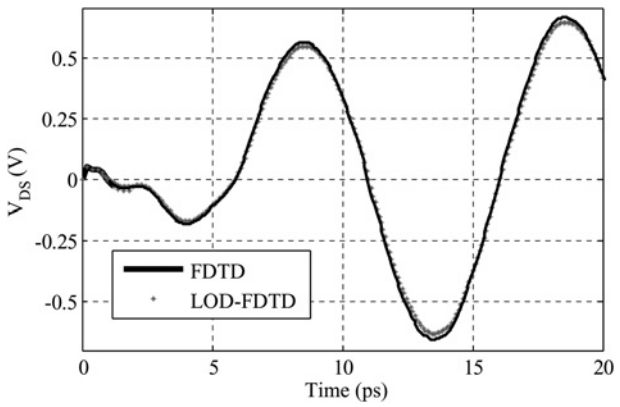

Fig. 14 *Output voltage of two-finger transistor*

source electrodes obtained by the integration on the output plane. The number of iterations for the conventional FDTD and LOD-FDTD methods are 2×106 and 2×103, respectively. On a Pentium-iv 2.50-GHz pc, it took about 1 s to finish the simulation of each time step with the conventional FDTD and 4.5 s with the LOD-FDTD method. Therefore a saving factor with the LOD-FDTD method in CPU time is about 220 when the conventional FDTD is used as a reference.

5 Conclusion

This work proposed an implicit LOD-FDTD method for the full-wave simulation of time-dependent semiconductor device equations in a very lower calculation time in comparison with the conventional explicit FDTD method. As the method is implicit, the time-step size can be increased up to a value that the numerical dispersion accuracy remains acceptable. As the size of the local minimum cell in the computational domain (which is imposed by the Debye length) is much smaller than the wavelength, the error limitation is larger than the CFL limitation. Therefore the full-implicit method is more efficient than the conventional explicit FDTD method for the full-wave simulation of active microwave/millimeter-wave devices. The performance of this new method was evaluated with two examples by presenting comparisons between the explicit, ADI- and LOD-FDTD methods.

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