A DC to 20 GHz Ultra-Broadband High-Gain-Linear Distributed Power Amplifier with 19.5% Drain Efficiency

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***Abstract*— In this paper an ultra-broadband linear distributed power amplifier (DPA) is presented. This amplifier consumes only 100 mW DC power and amplifies input powers up to -3.7 dBm with a power gain of 16.7 dB linearly. Output power at 1-dB compression point is 13 dBm in the linear-mode. By increasing the level of input power, the amplifier no longer works in the linear-mode, drain efficiency and non-linear distortions are increased, and power consumption is decreased to 90 mW. S_{21} parameter is 18±0.9 dB over DC to 20 GHz. The architecture of all power gain cells (including three stages) is cascade of inductively coupled common source. This amplifier is simulated in a 0.13 um CMOS technology.**

Keywords- distributed amplifier; ultra-broadband; cmos technology

I. INTRODUCTION

There is a trade-off between frequency bandwidth and power gain of a PA in both wired and wireless communication systems. Meanwhile, the amount of noise presented in existing systems, decrease channel capacity [1]. To overcome the coming noise effect and then constructing an immune system, the frequency bandwidth and transmitted power should be desirably increased. By increasing frequency bandwidth or transmitted power, data rate would be also increased in an immune way [1]. Radiography systems gain special data of an object by sending and receiving waves over a wide-bandwidth. Therefore, a complete recognition of the object is available by radiography. On the other hand, an increasing demand of sending data with high rates has increased the design of wide-band systems. As a result, design and fabrication of wide-bandwidth transceivers is an interesting problem to RF circuit designers.

The most important part of a transceiver is power amplifier (PA), which has an intrinsic role in supporting wide-bandwidth as well as high gain. The most proper concept to increase frequency bandwidth is distributed amplifier structure . Until now, many papers have been reported in which distributed voltage amplifiers have been designed and manufactured [3-7].

In this paper, a DC to 20 GHz ultra-broadband distributed power amplifier (DPA) is presented. This class-A DPA has a power gain of around 16.7 dB and PAE of 19.5% while delivers output power of 13 dBm at 1-dB compression point to a 50 Ω load. The technology foundation used to simulate this DPA is 0.13 um CMOS.

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II. CIRCUIT ANALYSIS

Single stage linear PAs are categorized into four classes: A, AB, B, and C based on duty cycles of their drain currents. Different duty cycles are made by altering input DC bias voltage [8].

However, class-A PAs have the least drain efficiency, but their high output power (higher power gain for a constant input power) and highest linearity are interested in this work.

Owing to the limited output power of a single sage PA, parallel power combining is the best idea to support high output power, as though, power losses due to the N-way power dividers and combiners makes it less practical [9]. On the other hand, distributed amplification technique is used to increase frequency bandwidth, could also solve the power losses of N-way paths at input/output of parallel power dividing/combining. Furthermore, every single amplification stage in a distributed power amplifier (DPA) should linearly amplify signals and then distributed amplification theory and artificial transmission line analysis can be applied.

A DPA absorbs the input and output parasitic capacitances of the gain cell (which have the main role to limit the bandwidth) into transmission line like structures which form a high order LC ladder filter, while combining gain in an additive fashion.

Fig. 1 shows a basic distributed amplifier. A distributed amplifier consists of a gate line and a drain line implemented either by artificial transmission lines (comprising of cascade of LC filter sections to form a ladder type structure) or by uniform transmission lines.

The characteristic impedance of these transmission lines and its phase velocity can be found, respectively, as

$$Z_0 = \sqrt{\frac{L}{C}}, v_P = \sqrt{LC} \quad (1)$$

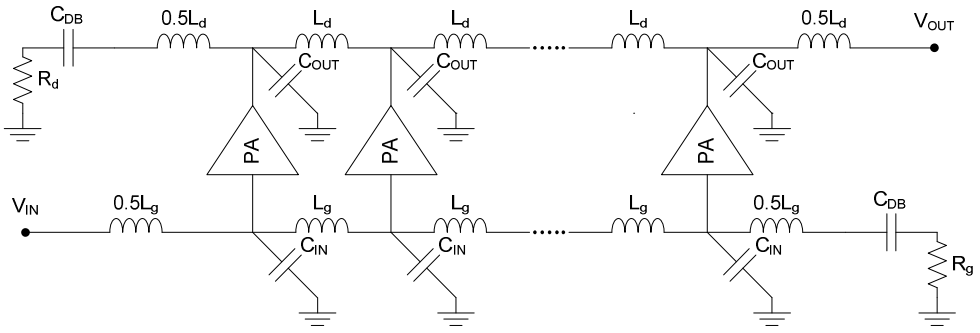

Fig. 1: A common architecture of a DPA

For $f<<fc$, where fc is the cut-off frequency of the artificial transmission line, which normally determines the bandwidth of the distributed amplifier, given as

$$f_C = \frac{1}{\pi\sqrt{LC}} \tag{2}$$

These two lines are coupled via active devices (transistors). The operation of a distributed amplifier is based on the fact that the signal from the input travels forward (towards the right in Fig. 1) along the gate line and gets amplified by each transistor. The drain line carries these amplified signals both in the forward and reverse direction. The forward travelling-waves on the drain line are in phase synchronization with the forward travelling wave of the gate line and with each other, implying that each device adds power in phase to the output signal at each tap point on the drain line. The forward travelling-wave on the gate line and the reverse travelling-wave on the drain line are absorbed by terminations which are generally matched to the loaded gate and drain lines.

The gain G of the conventional distributed amplifier has been analyzed in [10] and can be estimated, in a loss-free case, by

$$G = \frac{n^2 g_m^2 Z_{0g} Z_{0d}}{4} \tag{3}$$

where n is the number of the stages, g_m is the trans-conductance of the each gain cell, and Z_{0g} and Z_{0d} are the characteristic impedance of the input line and output line, respectively.

Equations (1), (2), and (3) work well when each gain cell in the PA topology of Fig. 1 amplifies input signal linearly. To support this idea, all gain cells should be operated in Class-A. Fig. 2 shows our used gain cell in this work that is a cascaded stage of two NMOS transistors. In this figure, two transistors are coupled via an interposed peaking inductor L. The gate of the upper transistor is terminated by resistor R. As a result, three poles are located on S-plane [11]. One pole which determines low frequency response is observed by resistance R and the input capacitance of the upper transistor. Two other poles, which are complex conjugate and located on the left side of the complex axis, are observed by peaking inductance L and the output capacitance of the lower transistor C_{OUT}. Then, the cut-off frequency of the gain cell G_m is considered as $1/\sqrt{LC_{out}}$ [11].

Thus, the overall cut-off frequency of DPA is affected by two types of pole: transmission line pole and G_m pole. But the dominant pole and then the cut-off frequency of DPA is determined by G_m pole [11]. Besides, gain flatness over a high bandwidth is achieved by selecting R and L properly.

Power gain (G_P) flatness is important instead of voltage gain flatness in DPAs in which G_P is calculated as [12]

$$G_P = \frac{1}{1-|\Gamma_{IN}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{4}$$

Furthermore, distributed amplifiers have well matched input-output as well as nearly flat gain (S_{21} parameter) over ultra-broad-bands. It sounds that S_{11}, S_{22}, S_{12}, Γ_{IN}, and Γ_{OUT} parameters of these amplifiers are small enough. So, we can neglect both first and third multiplying terms in (4) and if the load and source impedances are equal then G_P can be approximated as (5). As a result, frequency bandwidth is considered by either S_{21} or G_P.

$$G_P \cong |S_{21}|^2 \tag{5}$$

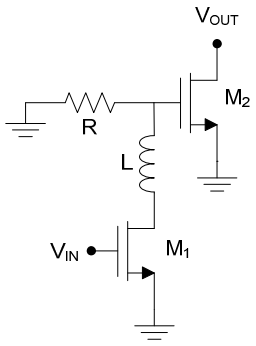

Fig. 2: The structure of the power gain cell (PA) in Fig. 1.

G_P in decibel form is expressed as $10\log(|S_{21}|^2)$ which equals $20\log(|S_{21}|)$ that is S_{21} in decibel form. Under this circumstance, S_{21} result is used to present power gain approximately.

III. Simulation & Results

Simulation results are generated by ADS (Advanced Design System) software. The technology foundation is 0.13 um CMOS. The value of n, the number of the stages, is 3.

The optimum values of L and R to get a flat power gain and ultra-broad-bandwidth are 1 nH and 80 Ω, respectively. Actually, the frequency response of DPA has a peaking frequency at the cutoff frequency. More/Less values of inductance L decrease/increase the cutoff frequency and increase/decrease the peaking frequency. In both cases, flatness is degraded. More values of resistance R increase power gain as well as peaking frequency. Therefore, linearity and flatness are degraded. Meanwhile, more values of resistance R increase cutoff frequency, decrease input impedance, degrade matching and decrease power gain. The inductor L would be manufactured as spiral.

However, the optimized source and load impedances are something other than 50 Ω [9], using standard characteristic impedance of 50 Ω obviates input and output matching networks and the presented DPA is directly connected to the prior block and antenna, in order to reduce chip area. Fig. 3 shows 50 Ω input and output matching. S_{11} and S_{22} parameters are better than 10 dB up to 20 GHz.

Power supply is 1.8 V. Gate bias voltages of both transistors and drain bias voltage of the lower transistor are 0.7 V. This amplifier draws 55 mA from 1.8 V power supply to deliver 20 mW output power to the 50 Ω load. This power is obtained from simulation at 1-dB compression point which is the maximum output power of amplifier in the linear-mode and has drain efficiency and PAE of 19.7% and 19.2%, respectively. Input power at 1-dB compression point is -3.7 dBm.

Due to the high gain of the circuit, the level of the incoming signal to the gate of the lower transistor at 1-dB compression point (-3.7 dBm) is low and it can be directly connected to up-converting mixers. Whereupon, the gate bias is remained at V_{TH} level and all lower transistors work in the linear region [13].

By increasing gate width of each transistor, output current is increased and then output power is increased. On the other hand, input capacitance is increased, input impedance is decreased, the loading effect of the present stage to the prior stage, and then input power is increased. To obtain maximum power gain, the optimized gate width for all transistors is 57 um that is a trade-off between input power and output power.

S_{21} parameter shown in Fig. 4 has a flat gain of 18±0.9 dB and the Isolation is better than 30 dB (Fig. 4) over a frequency range of DC to 20 GHz. By considering input and output return losses in Fig. 5, we can use (5) and then power gain as approximately the same as S_{21} parameter.

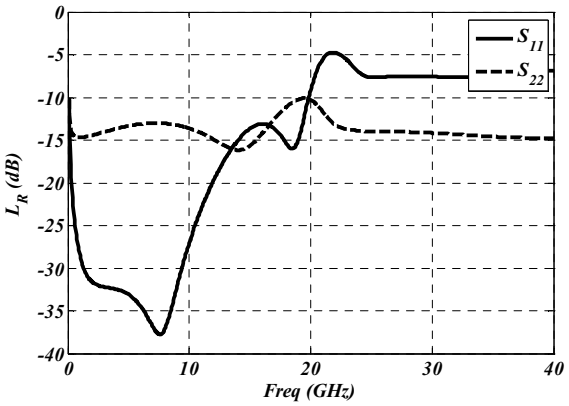

Fig. 3: Input and output return losses.

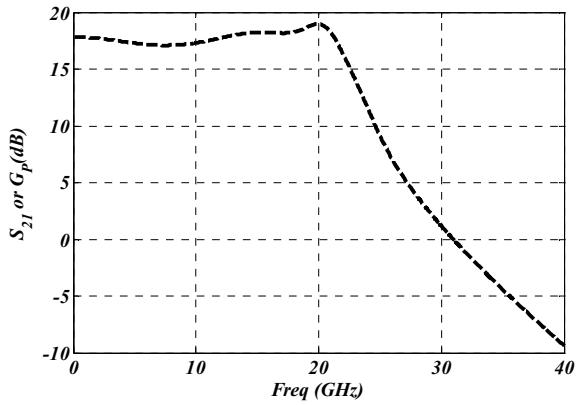

Fig. 4: S_{21} parameter

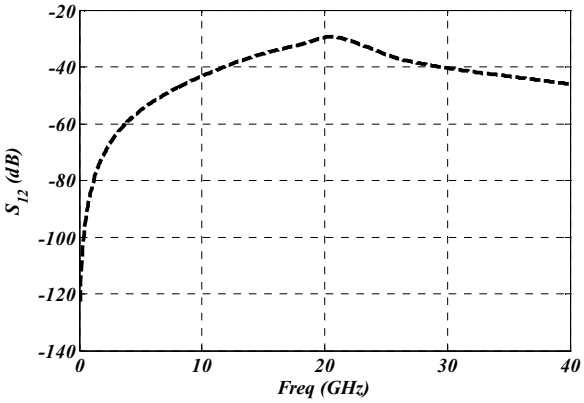

Fig. 5: Input and output Isolation

If input power is increased more than -3.7 dBm then amplifier works with a duty cycle of less than 360º and class-A amplification moves towards class-AB or class-B amplification. As it has shown in Fig. 6, drain efficiency is increasing up to 36% at input power of 9 dBm. On the other hand, linearity is decreased and OIP3 is degraded from 22.4 dB to 15.6 dB (Fig. 7).

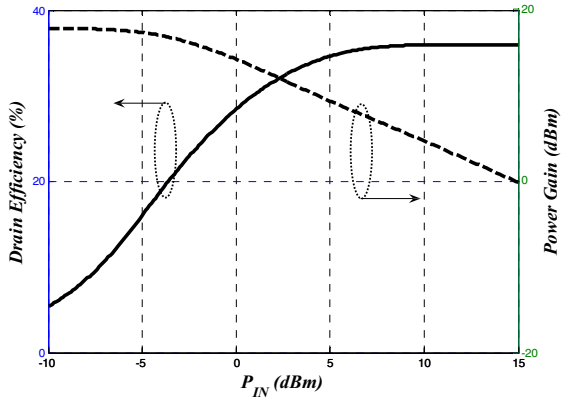

Fig. 6: Drain efficiency and power gain versus input power

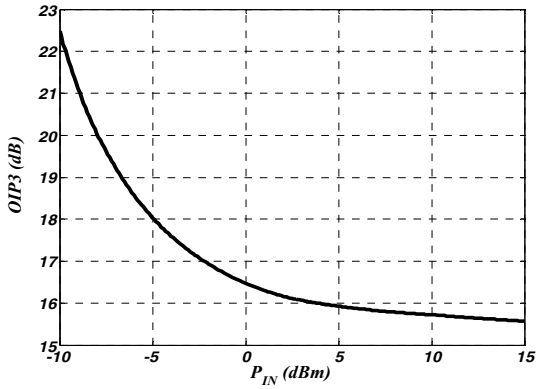

Fig. 7: Third-order-intercept point versus input power

IV. CONCLUSION

An ultra-broadband DPA has been presented. Using distributed technique, output powers of power gain cells are combined without using multi-way power combiner. Amplifier has a well matched input-output that helps us to use the simulation results and analysis of the distributed voltage amplifier for the presented DPA. This PA is directly connected to the output 50 Ω load, and hence there is no need to the matching network.

The validity of the design was demonstrated by simulation of our DPA with a 0.13 um CMOS technology.

The DPA works in the linear-mode for input powers of less than -3.7 dBm and a power gain of about 16.7 dB. Input powers of more than -3.7 dBm caused DPA to include duty cycles of less than 360º and delivered maximum output power of 30 mW with drain efficiency of 35.7% to the 50 Ω load.

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